Simulation of 0.35um CMOS process and device use Silvaco TCAD tools

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1. Introduction

Silvaco TCAD tools provide accurate prediction for both process simulation and device simulation. This article presents a 0.35um CMOS flow from process to device via simulation tool of Silvaco products. The process recipes and fabrication flows are referred from University of California, Berkeley Micro lab open resource. The first chapter covers pure process part which use Silvaco process tool Athena, second chapter performs device simulation (Atlas) and displays fundamental device characteristics.

2. process simulation

Silvaco process tool (Athena) emulates standard wafer Fab flow from mask layout (GDS) to carry the rest consequence processes. Firstly, a GDS layout (Figure2-1) contains a pair of minimum feature sized (L=0, 35um, W=5.0um) NMOS and PMOS is captured and loaded (Figure2-2).

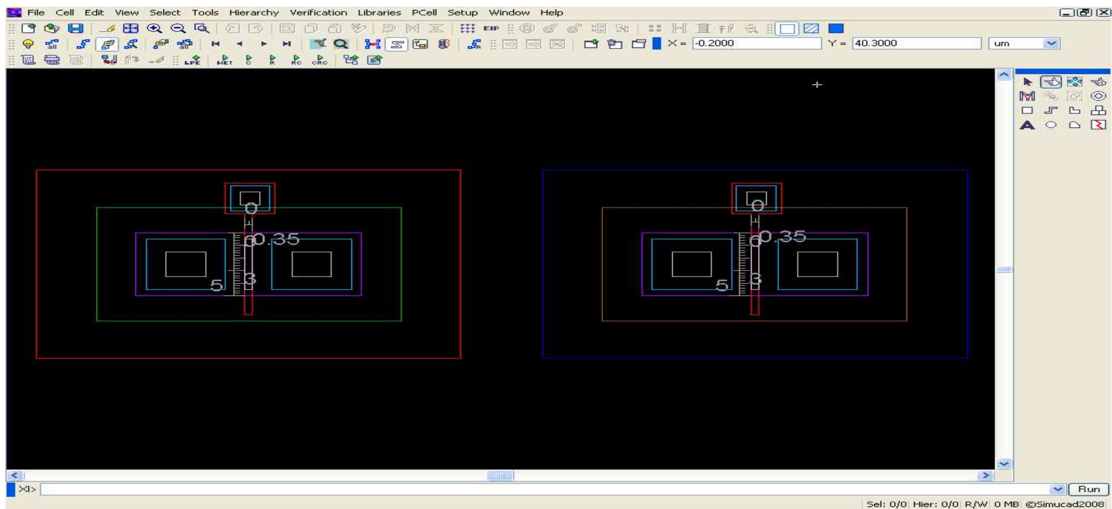

Figure2-1

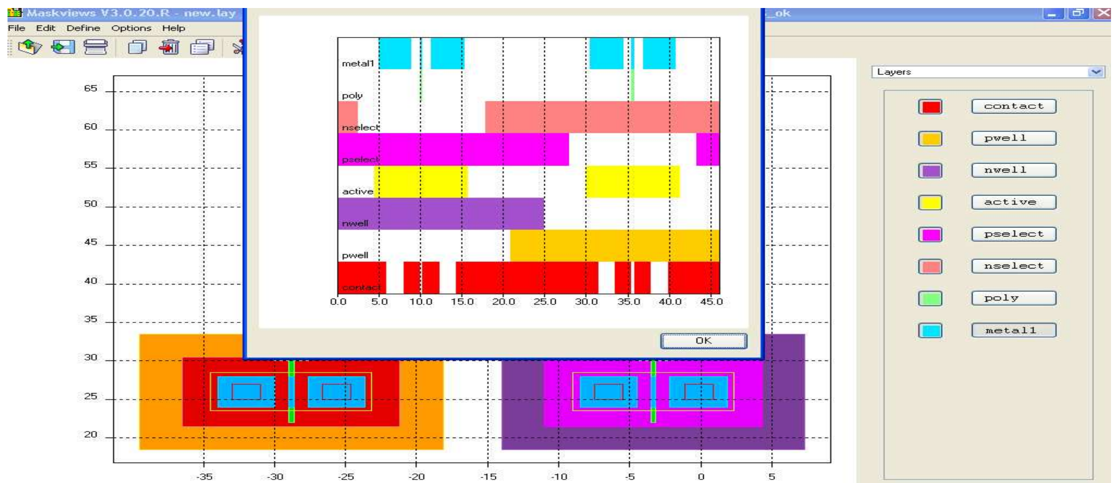

Figure2-2

The layout file is streamed out and loaded in Maskviews (Figure2-2), and then a proper cutline is generated after loading GDS format layout.

Once the layout and cutline file is loaded in Athena, the following process steps (Figure2-3) are carried on in DeckBuild.

Step 0. Starting wafers	Step 33. N-type LDD implant photo
Step 1. Initial oxidation	Step 34. N-type LDD implant
Step 2. Zero layer photo	Step 35. LDD spacer deposition
Step3. Zero layer etch	Step 36. LDD spacer etch
Step 4. Pad oxidation/nitride deposition	Step 37. P+ gate and S/D photo
Step 5. N-well photo	Step 38. P+ gate and S/D implant
Step 6. Nitride etch	Step 39. N+ gate and S/D photo
Step 7. N-well implant	Step 40. N+ gate and S/D implant
Step 8. Nitride removal	Step 41. Backside etch
Step 9. Pad oxidation/nitride deposition	Step 42. Gate and S/D annealing
Step 10. P-well photo	Step 43. Silicidation (Ti)
Step 11. Nitride etch	Step 44. PSG dep. and densification
Step 12. P-well implant	Step 45. Contact photo
Step 13. Nitride removal	Step 46. Contact etch
Step 14. Well drive in	Step 47. Metal 1 deposition
Step 15. Pad oxidation/nitride deposition	Step 48. Metal 1 photo
Step 16. Active area photo	Step 49. Metal 1 aluminum etch
Step 17. Nitride etch	Step 50. Sintering
Step 18. P-well field implant photo	Step 51. Testing
Step 19. P-well field ion implant	Step 52. Dielectric deposition/planarization
Step 20. LOCOS oxidation	Step 53. Via 1 Photo
Step 21. Nitride and pad oxide removal	Step 54. Via 1 Etch
Step 22. Sacrificial oxidation	Step 55. Metal 2 deposition
Step 23. Screen oxidation	Step 56. Metal 2 photo
Step 24. NMOS Vt adjust. implant photo	Step 57. Metal 2 etch
Step 25. NMOS Vt adjustment implant	Step 58. Testing
Step 26. PMOS Vt adjust. implant photo	Step 59. Dielectric deposition/planarization
Step 27. PMOS Vt adjust. implant	Step 60. Via 2 photo
Step 28. Gate oxidation, poly-Si dep.	Step 61. Via 2 etch
Step 29. Gate photo	Step 62. Metal 3 deposition
Step 30. Poly Si etch	Step 63. Metal 3 photo
Step 31. P-type LDD implant photo	Step 64. Metal 3 etch
Step 32. P-type LDD implant	Step 65. Testing

Figure2-3

Above detailed process steps and recipes are referred and quoted from University of California Berkeley Micorlab public technical report. Author slightly converted and modified few process steps and parameters.

Some key process steps and results matches experiment measurement data. Below pages demonstrate a few simulation results. Figure2-4 is oxide thickness (Tox) extracted and measured after certain process step obtained in Athena. Simulated Tox is roughly achieved 7.45nm which is quite closer to experimental data (7.5nm).

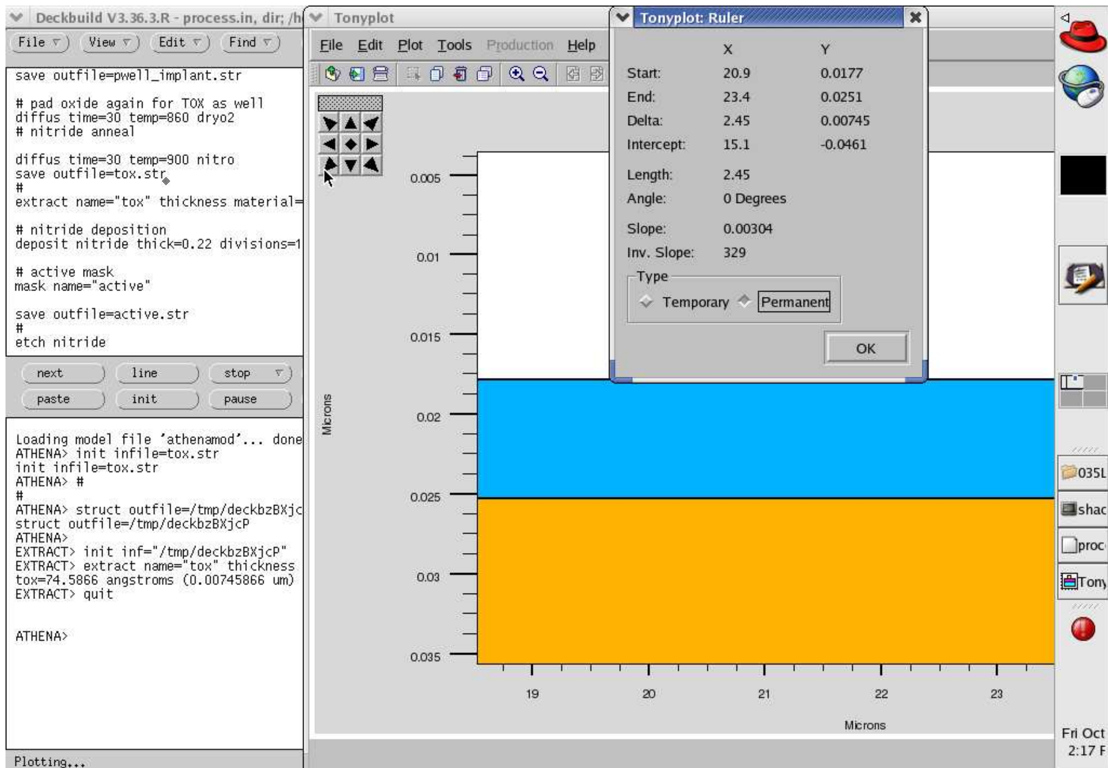

Figure2-4

Each junction depth in respect to NMOS SD, PMOS SD and NWELL. (Figure2-5)

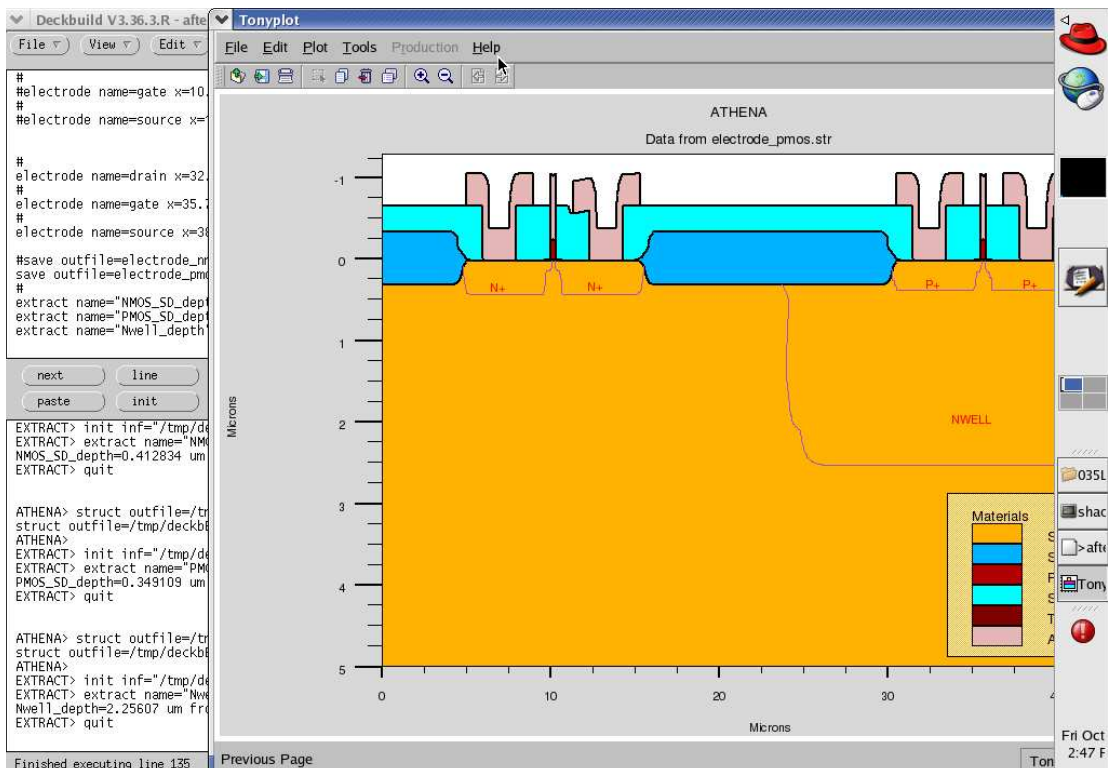

Figure2-5

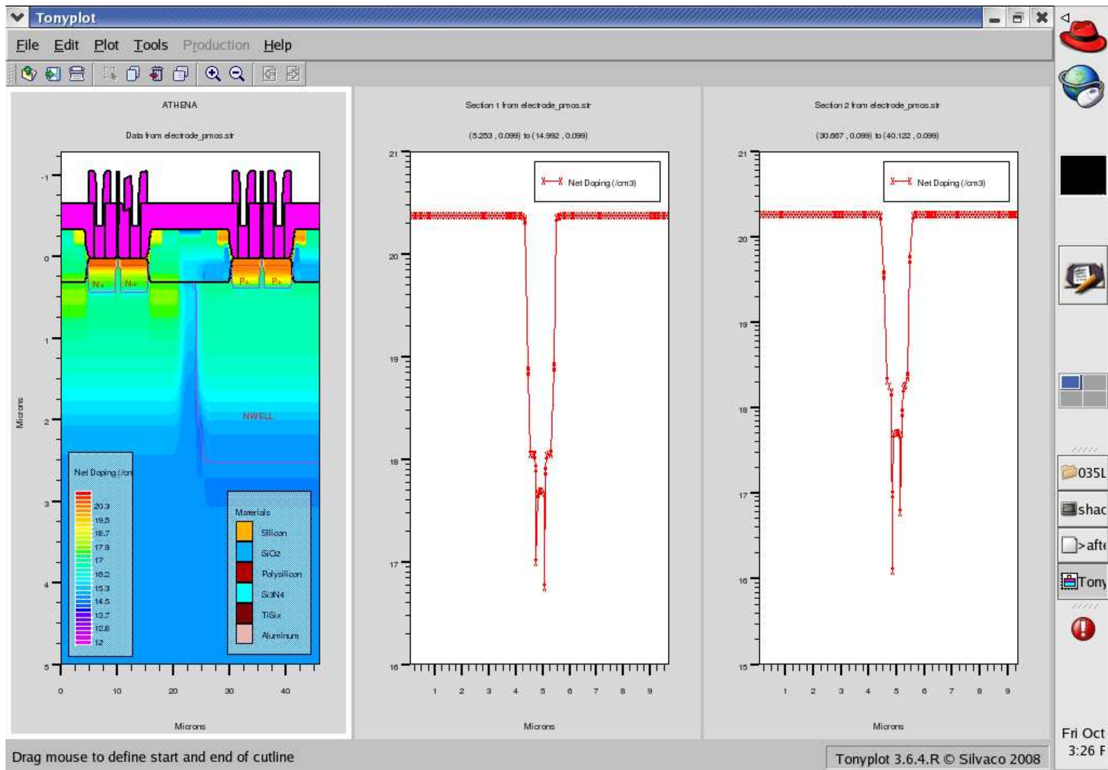

Figure2-6 final process structure and doping profile cutline beneath gate oxide

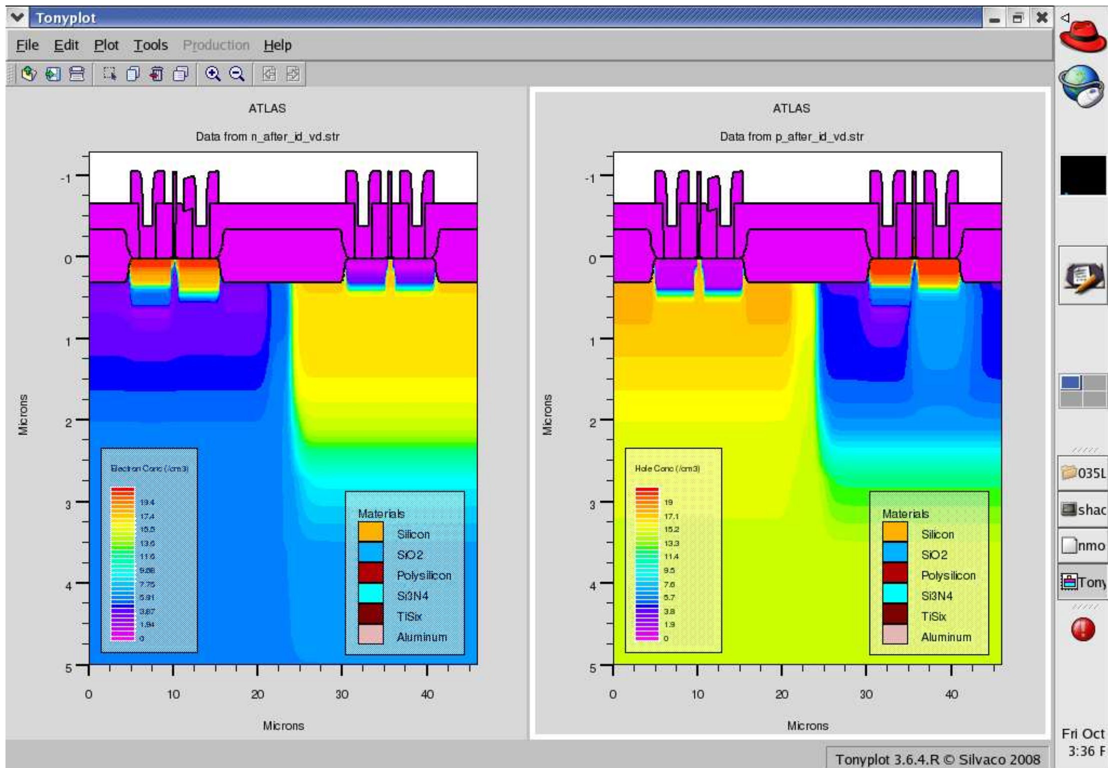

Figure2-7 Electron and Hole concentration table

3. Device simulation

Device simulation follows previous completed process structure, a special customized version Atlas is used due to large nodes exceed the limits of ordinary version Atlas.

DC analysis

Both NMOS and PMOS performed DC simulation with each biasing conditions. NMOS starts the ID_VG (Figure 3-1) simulation with a slight DC voltage applied at drain electrode contact 0.05V (VDS=0.05), the gate ramps from 0V to 4V with a step size 0.1. Substrate voltage varies from 0v to -3v with a step size -1v.

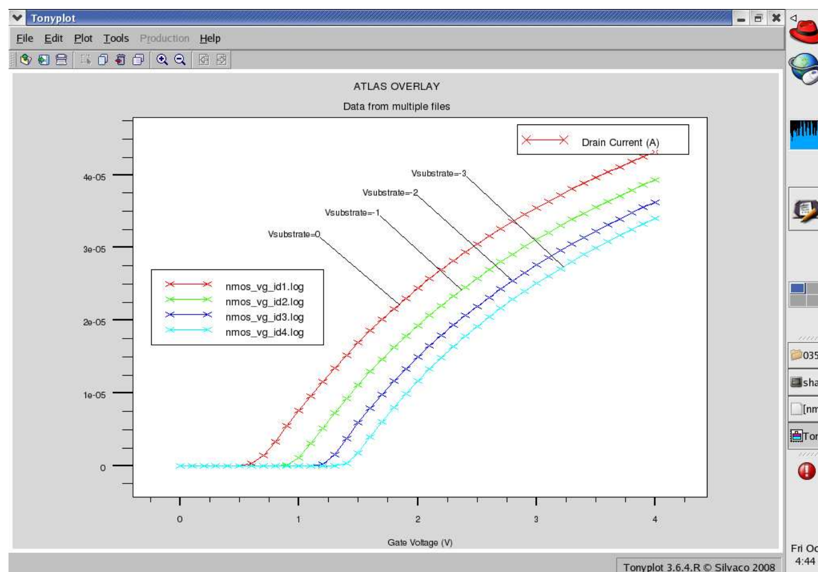

Figure 3-1

NMOS ID_VD (Figure 3-2) varies different gate voltage from 1 to 4V then ramp the drain voltage from 0 to 4V with a step size 0.1V.

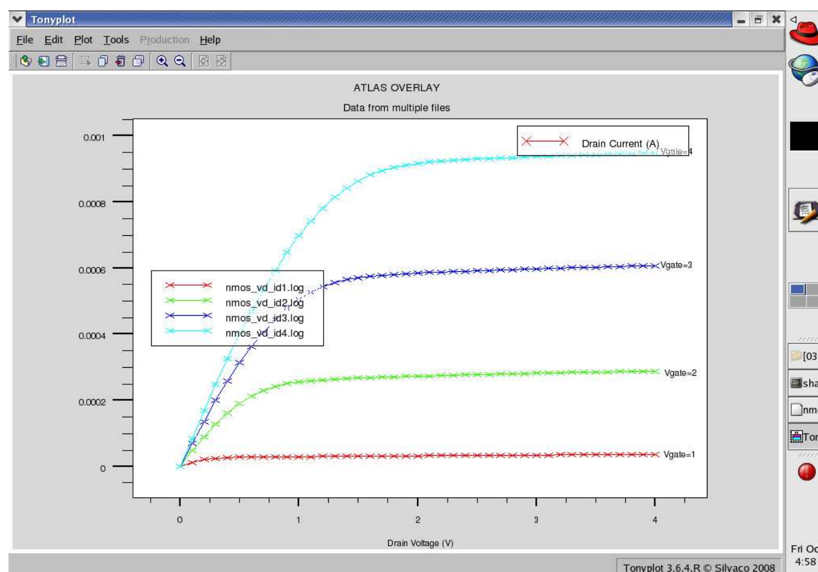

Figure 3-2

Finally, a few DC parameters (Figure 3-3) are extracted after DC simulation for NMOS.

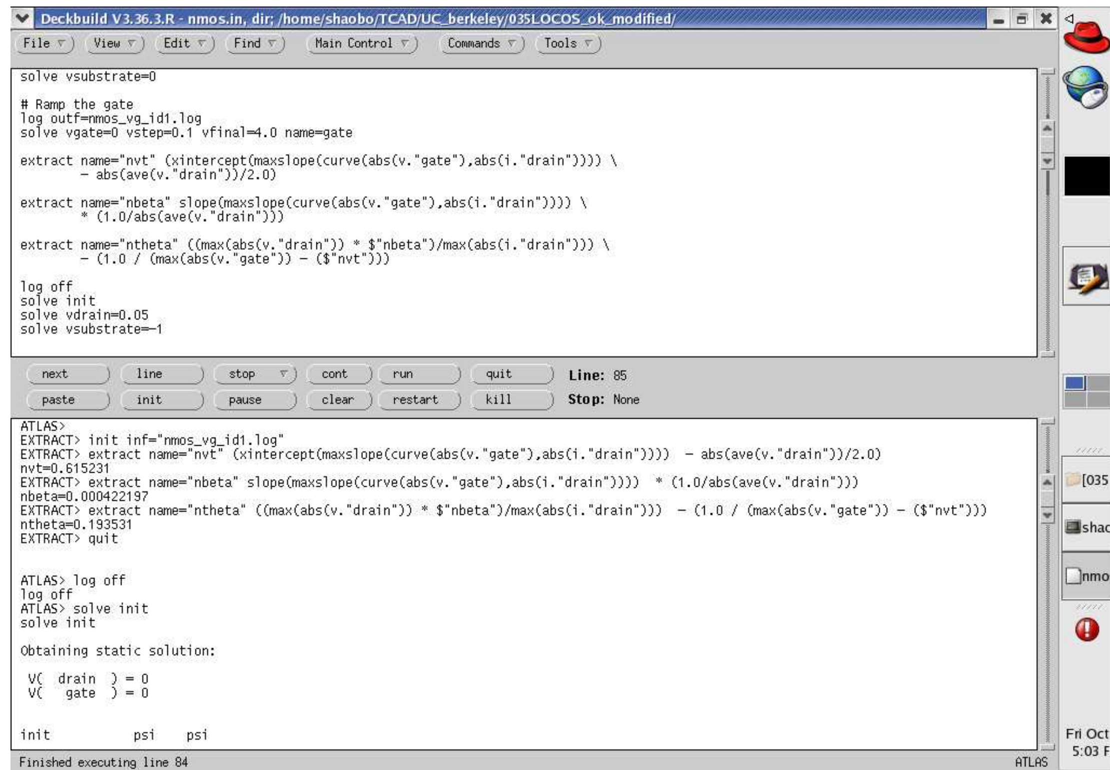

Figure 3-3

Similarly for PMOS device, ID_VG (Figure 3-4) and ID_VD (Figure 3-5) curves are simulated.

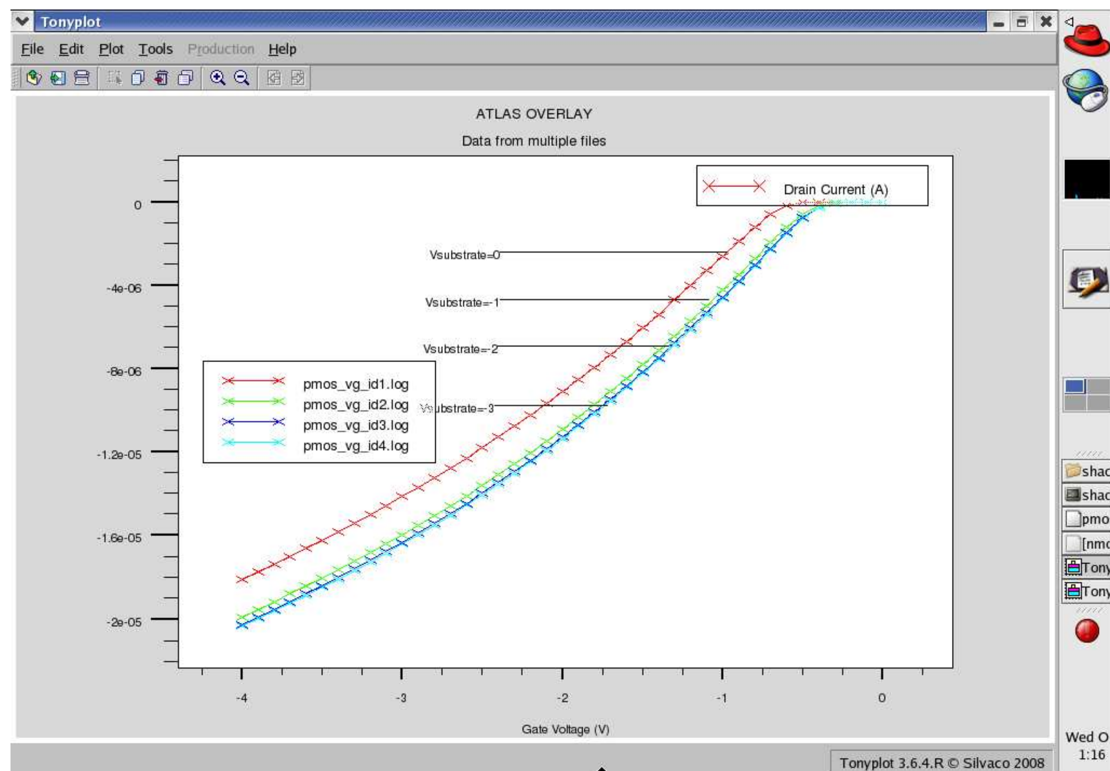

Figure 3-4

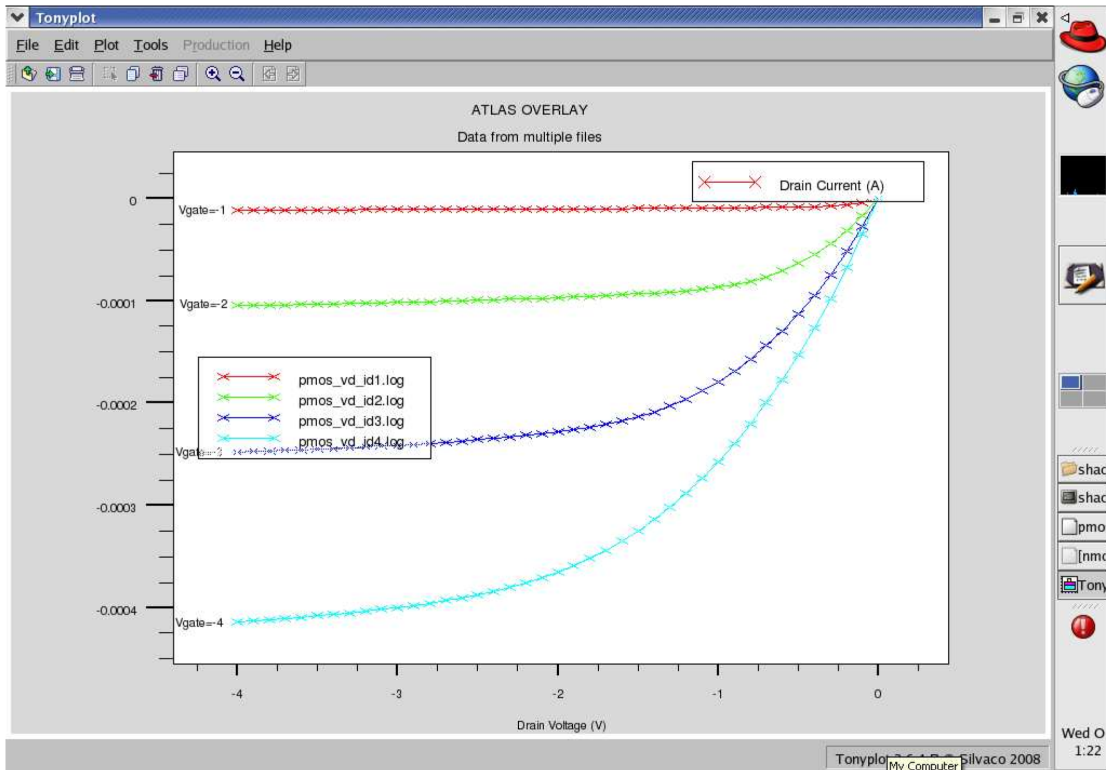

Figure 3-5

```
Deckbuild V3.36.3.R - pmos.in, dir; /home/shaobo/TCAD/UC_berkeley/035LOCOS_ok_modified/
File  View  Edit  Find  Main Control  Commands  Tools

solve vdrain=0 vstep=-0.1 vfinal=-4.0 name=drain

log off
solve init
solve vgate=-0.1
solve vgate=-0.5
solve vgate=-0.8
solve vgate=-1
solve vgate=-1.5
solve vgate=-2
solve vgate=-2.5
solve vgate=-3
solve vgate=-3.5
solve vgate=-4
log outf=pmos_vd_id4.log
solve vdrain=0 vstep=-0.1 vfinal=-4.0 name=drain
save outfile=p_after_id_vd.str
tonyplot -overlay pmos_vd_id1.log pmos_vd_id2.log pmos_vd_id3.log pmos_vd_id4.log

next  line  stop  cont  run  quit     Line: 110
paste init  pause clear restart kill  Stop: None

Total time:          872.23 sec.

ATLAS>

ATLAS>
EXTRACT> init inf="pmos_vg_id1.log"
EXTRACT> extract name="pvt" (xintercept(maxslope(curve(abs(v."gate"),abs(i."drain")))) - abs(ave(v."drain"))/2.0)
pvt=0.61292
EXTRACT> extract name="pbeta" slope(maxslope(curve(abs(v."gate"),abs(i."drain"))))  * (1.0/abs(ave(v."drain")))
pbeta=0.000143023
EXTRACT> extract name="ptheta" ((max(abs(v."drain")) * $"pbeta")/max(abs(i."drain")))  - (1.0 / (max(abs(v."gate")) - ($"pvt")))
ptheta=0.100033
EXTRACT> quit


ATLAS> log off
log off
ATLAS> solve init
solve init

Obtaining static solution:

 V(  drain  ) = 0
Finished executing line 109                                         ATLAS
```

Figure 3-6 extracted DC parameters for PMOS

AC analysis

Both NMOS and PMOS ramps gate voltage from 0V to 4V and -4V to 0V with an AC signal 1MHz is applied in respect. The CV (capacitance-voltage) curve (Figure 3-7) plots relationship between gate and substrate region.

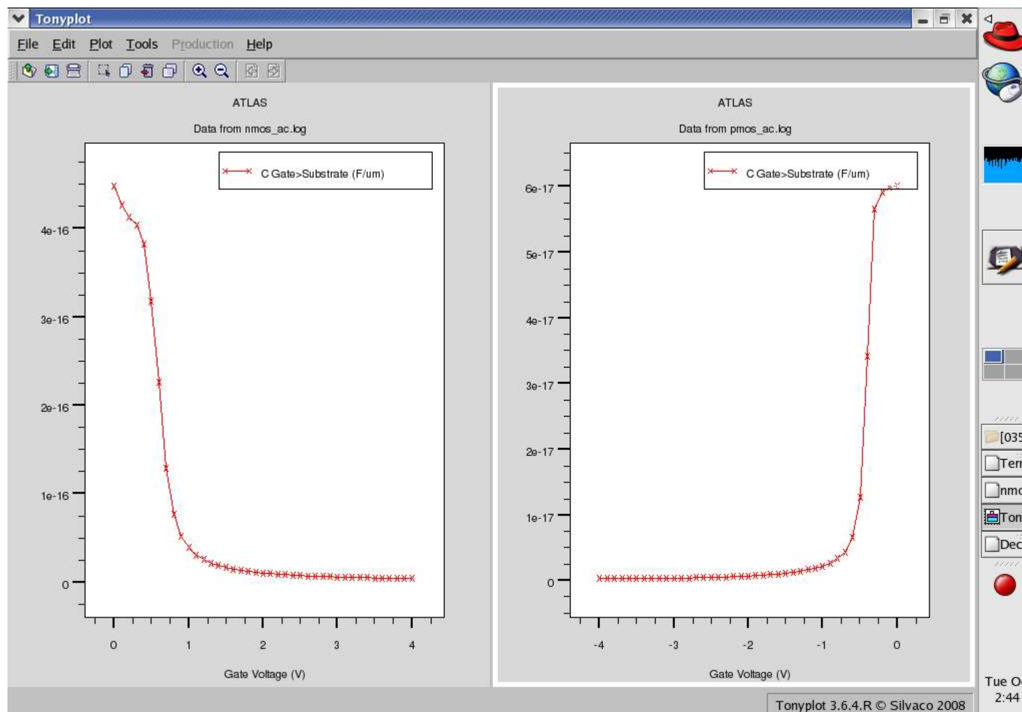

Figure 3-7

Additionally, a frequency domain AC simulation of S-parameters is calculated as a function of frequency from 10Hz to 50GHz. The S-parameters for NMOS and PMOS: S11 & S22 plain displays on a Smith Chart (Figure 3-8).

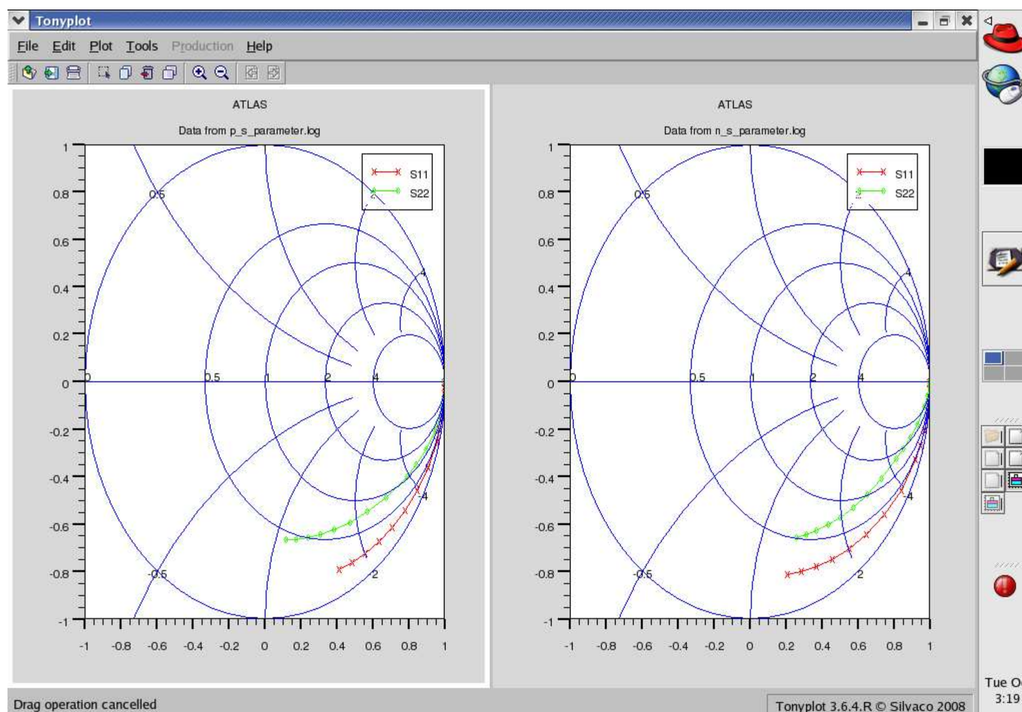

Figure 3-8

4. Conclusions

A complete 0.35um CMOS process is fabricated and simulated in Deckbuild using Silvaco process tool Athena. Each simulation process step follows table process recipes and conditions; the finial simulated process structure then is delivered to Atlas (device simulation) for device characterizations. DC and AC simulation results are obtained; the simulated IV data can be exported to third party modeling tools for performing device modeling.

References

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- Jones, S.K.; Bazley, D.J.; Beanland, R.; Badenes, G.; Scaife, B. "Simulation of Semiconductor Processes and Devices", 1997. SISPAD apos;97., 1997 International Conference on Volume , Issue , 8-10 Sep 1997 Page(s):185 – 188
- Burenkov, K. Tietzel and J. Lorenz "Optimization of 0.18 μm CMOS devices by coupled process and device simulation"
- Atlas user manual version 5.15.7.C