A case study of UMOS simulation from process to device with Silvaco tools

1. Introductions.

UMOS (U-shaped MOSFET) has supreme advantage, faster switching reposes, high input impedance and thermal reliability over traditional bipolar junction transistor. The application of UMOS device is emphasized not only power device but also high frequency (RF) circuits. Many foundries Fabs integrate UMOS characteristics into BCD (Bipolar CMOS DMOS) process flows. This article presents a simulation of a UMOS structure from process to device with Silvaco Athena (2D process) and Atlas (2D device and 3D device).

2. Process fabrication simulations.

Firstly, a two dimensional (2D) process flow (Figure 2.1) is being created with specified foundry recipes.

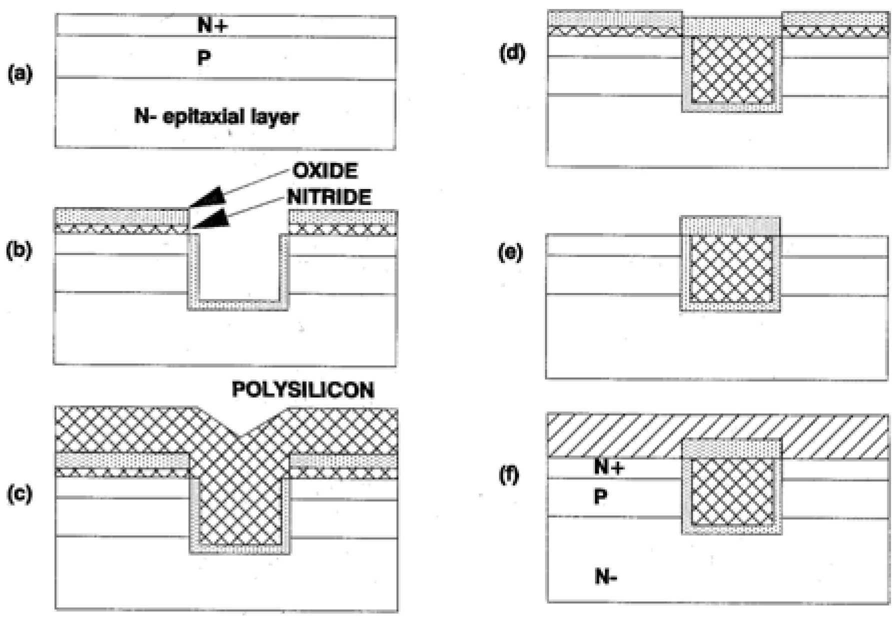

Figure 2.1

These process recipes provided from foundry are a generic case which may result different yielding, therefore calibration of individual process simulation steps have to perform to match it.

- Initially, an N-type silicon substrate is being defined and with a phosphorus doping concentration of 1e18cm-3.
- A 5um Epitaxy layer is growth on top of silicon substrate with 4e16cm-3 (approximately 0.15 ohm/cm) concentration phosphorus impurity doped.
- Then a RIE process is used to etch the silicon trench with a depth of 1.2um
- The dry oxidation process is then performed at 950C for 30min to grow a thin oxide layer of about 200 Angstrom on silicon surface.
- Polysilicon is then deposited and etched to form the trench polysilicon gate.

- P-Well is implanted with boron at 60KeV with a dose of 1.8e13cm-2
- P-Well Drive-In at 1150C for 30min
- N+ Source is formed by implanting Arsenic at 60KeV with a dose of 8e15cm-2
- Finally, the P+ buffer is form by implanting boron at 160KeV with a dose of 5e13cm-2

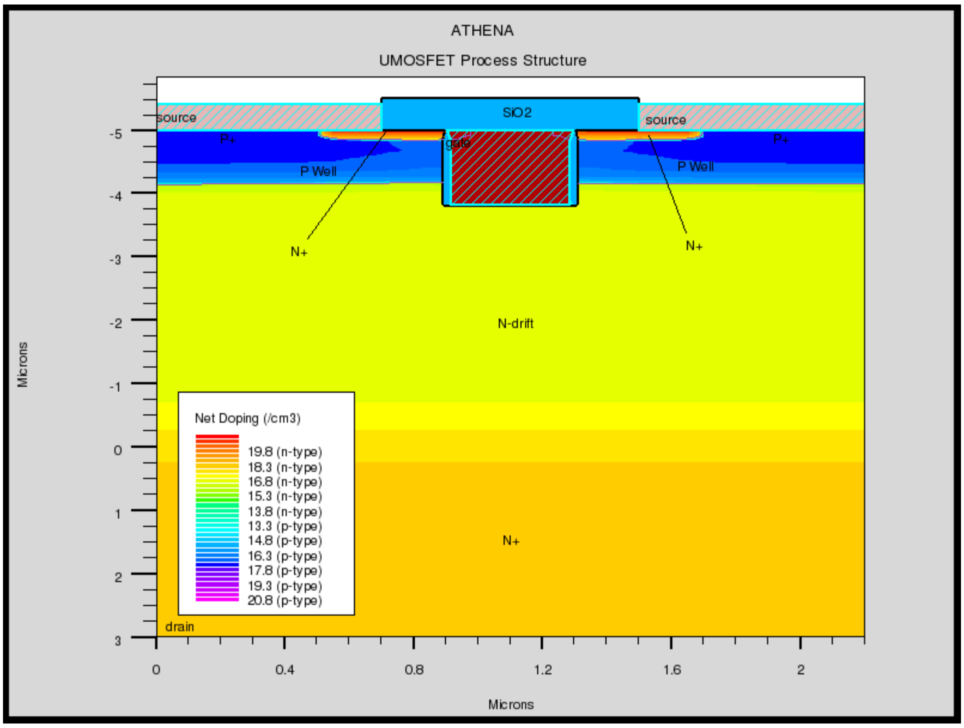

Figure 2.2

3. *Threshold voltage (Vth) calibration*

Key device parameter needs to be calibrated once the completed process structure (Figure 2.2) is done. The original threshold voltage obtained from Fab is about 1.9 V. P-Well, N+ Source and P+ buffer implantation plays very important effects on threshold voltage adjustment. Silvaco Deckbuild Optimizer is designed to match targeted result by verifying different user defined parameter variables such as (time, temperature, does, energy....etc). UMOS Optimizer (Figure 3.1) highlights target parameters of each P-Well, N+ Source and P+ buffer implantation. An extract statement must be defined whether process extraction or device extraction during optimization. The optimization procedure (Figure 3.2) is timing consuming and depend your process structure, it continues to calculate matrix equation till reaching the approximate target expectations (Figure 3.3).

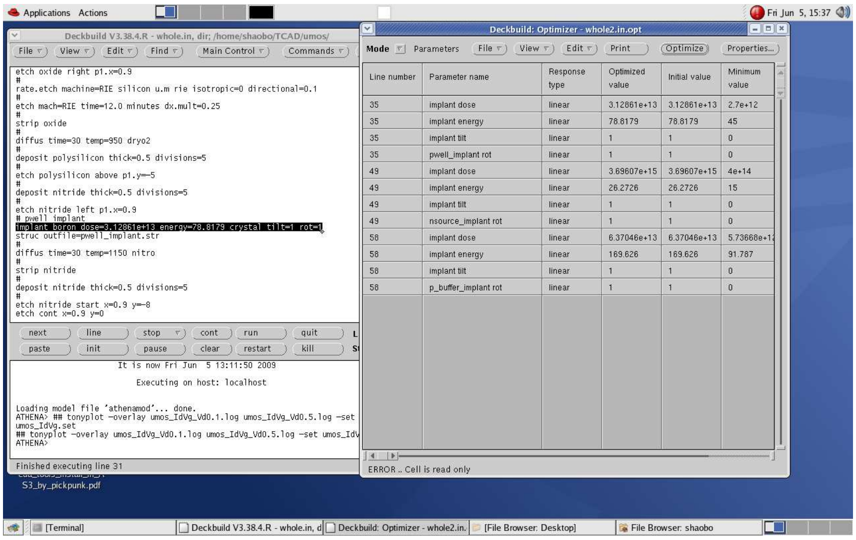

Figure 3.1

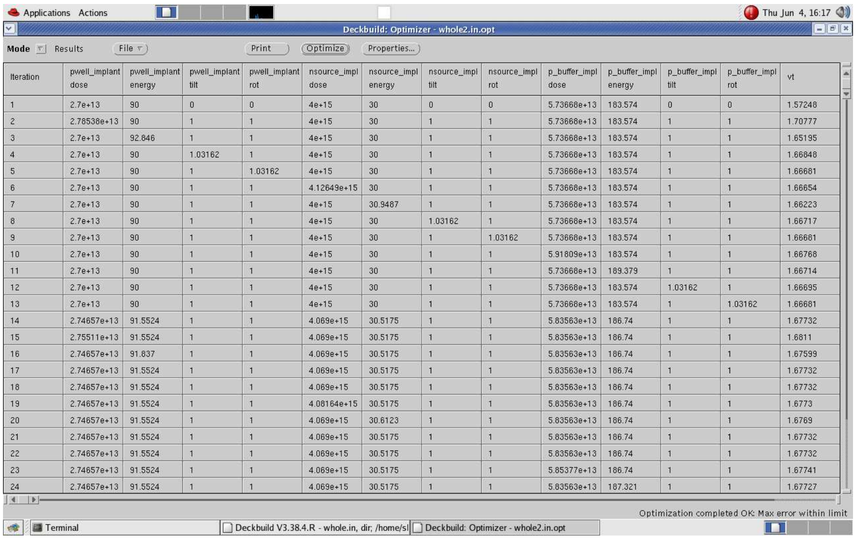

Figure 3.2

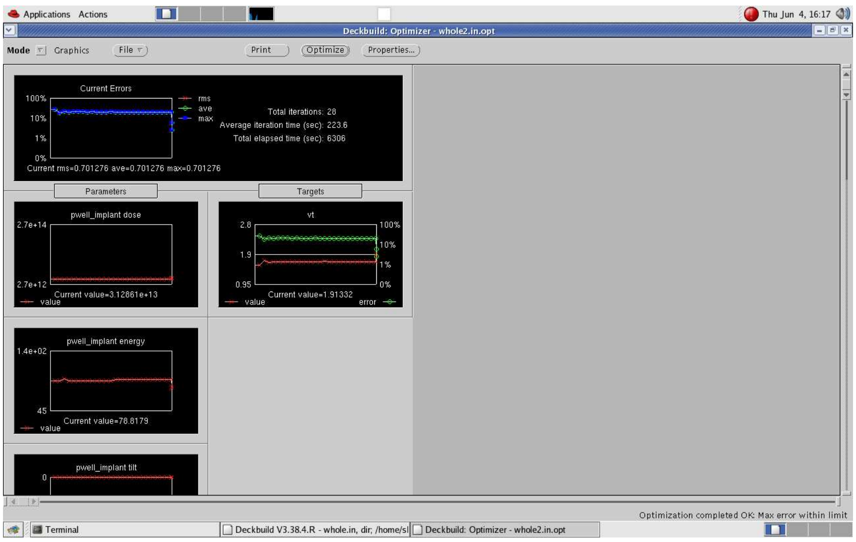

Figure 3.3

4. *Device simulations*

After threshold voltage calibration, we performed device testing which include DC basing in Atlas3D (Figure 4.1).

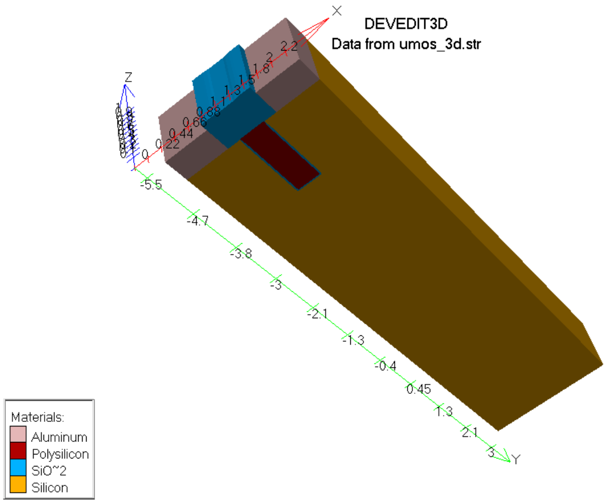

Figure 4.1

0.5 voltage is biased at drain terminal and then ramp the gate terminal from 0 voltage up to 12 voltage (Figure 4.2).

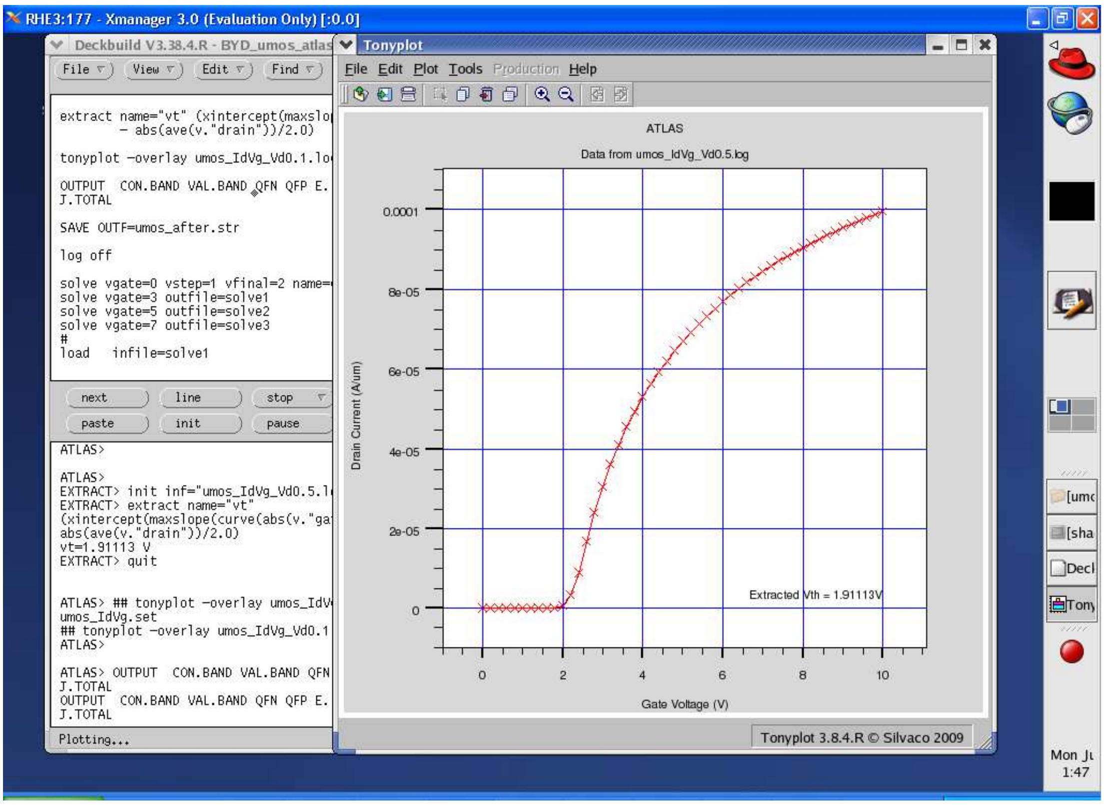

Figure 4.2 Ids vs Vgs

Similarly, Ids against Vds (Figure 4.3) is captured with different gate voltage applied and drain voltage ramped up to 20V.

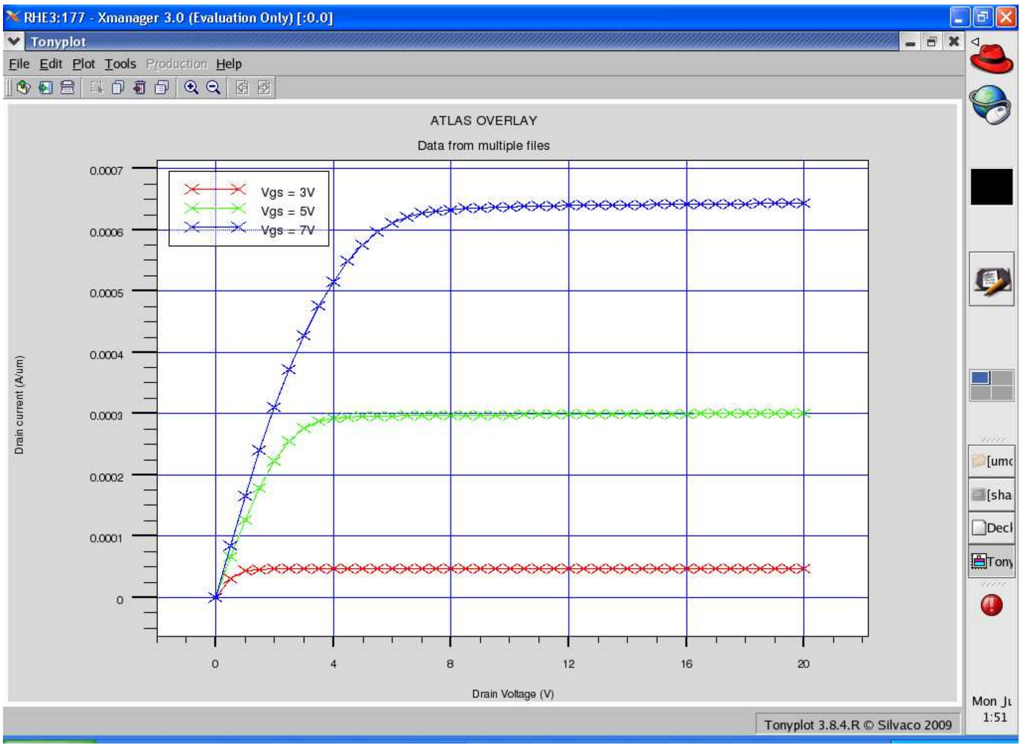

Figure 4.3

Few device characteristics (Figure 4.4) are plotted and saved after DC simulation. Below page displays electric field and current density surround gate terminal.

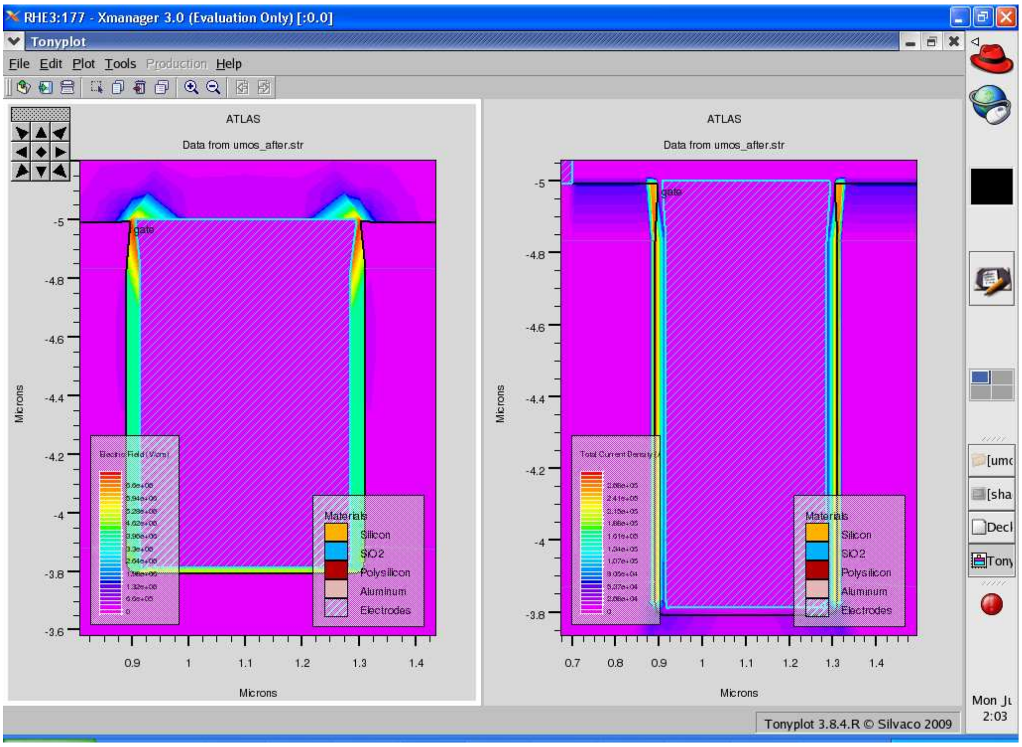

Figure 4.4

5. conclusions

A complete UMOS device structure is fabricated from process to device level via simulation tools Athena and Atlas. Threshold voltage calibration is achieved and device simulation results are obtained. Further investigation needs carry on such as higher channel density (W/L varies), specified on resistance study and break down voltage…etc