

Cadence mixed signal (SpectreVerilog) compatible simulation in Simucad AMS flow

Abstract

SpectreVerilog as Cadence mixed signal simulator embeds inside ADE (analog design environment), it is only suitable for small and medium size designs with good A2D and D2A interfaces. Simucad AMS (analog and mixed signals) provide alternative replacement tools in order to implement Cadence mixed signal design in Simucad AMS flow. The main purpose of this article demonstrates how Cadence mixed signal design can be implemented and re-designed in Simucad products.

Cadence design exportation

A practical PFD (phase frequency detector) mixed signal circuit is being constructed in Cadence ADE (Figure 1-1) with not only Schematic view (Spice) but also Functional view (Verilog) and veriloga view (VerilogA).

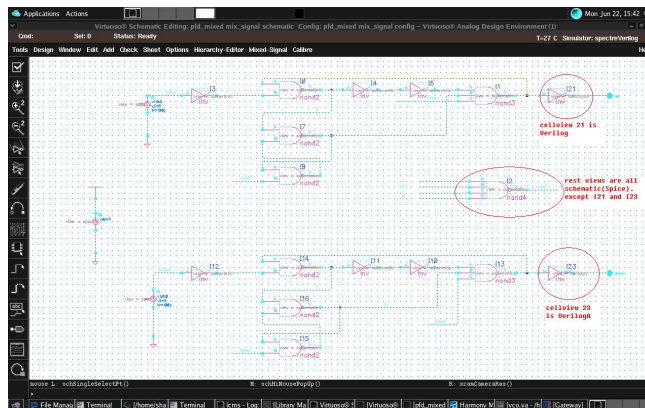


Figure 1-1

The config view (Hierarchy-Editor) must be implemented in order to perform mixed simulation once above (Figure 1-1) composer schematic view done. IE (interface element) setting keeps it as default value and ensures Functional and veriloga view displayed properly in Hierarchy-Editor (Figure 1-2).

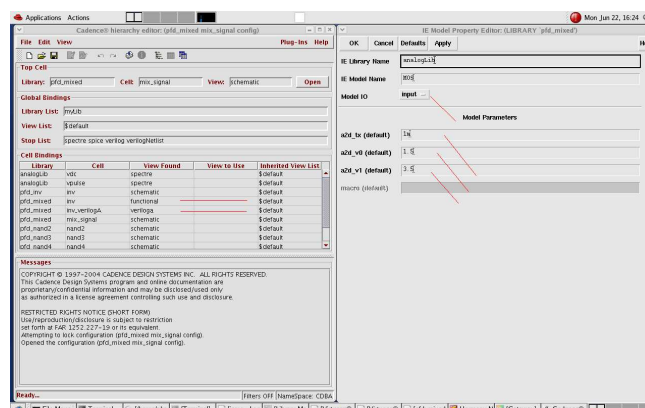


Figure 1-2

Simulation waveform (Figure 1-3) clearly indicates that up (verilog view) signal activated only when dclock is lagging data, down (veriloga view) signal activated only when data is lagging dclock.

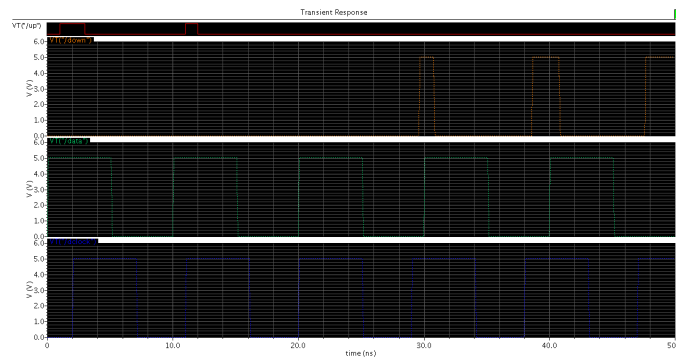


Figure 1-3

Then Cadence mixed signal schematic view is able to export (Figure 1-4) to Gateway (Simucad schematic editor) in EDIF 200 format after the functionality simulations.

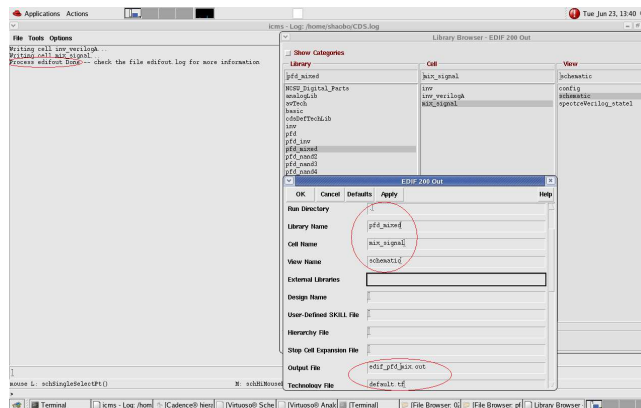


Figure 1-4

Simucad flow implementation

Copy Cadence exported EDIF (edif_pfd_mix.out) file into Gateway (Simucad schematic editor) working directory to import (Figure 2-1) it.

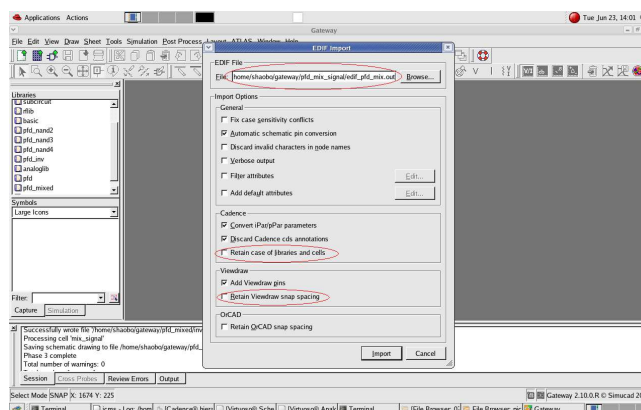


Figure 2-1

After Gateway successfully imports EDIF 200 file, slightly modify imported symbols in gateway to generate Spice netlist. Then we can modify the spice netlist from Gateway into a mixed signal netlist in Harmony (Simucad mix signal simulator). Below (Figure 2-2) demonstrates imported EDIF file from Cadence ADE and generation of Gateway schematic view and Smartspice (Simucad spice simulator) netlist

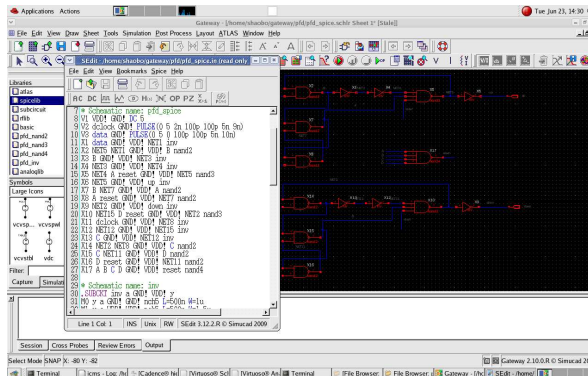


Figure 2-2

Once we get Spice netlist from Gateway, we need convert true spice netlist to mixed signal netlist in Harmony (Simucad mixed signal simulator).

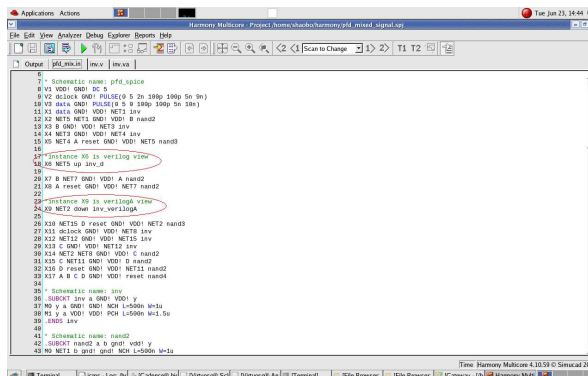


Figure 2-3

Instance X6 (Verilog) and instance X9 (VerilogA) is corresponding (Figure 2-3) to previous Cadence mixed signal schematic view I21 (functional view) and I23 (veriloga view) in respect. Module name of both Verilog and VerilogA must be in upper case (Figure 2-4). The module name of verilog and veriloga and Spice sub-circuit name also must match to instance in Harmony syntax.

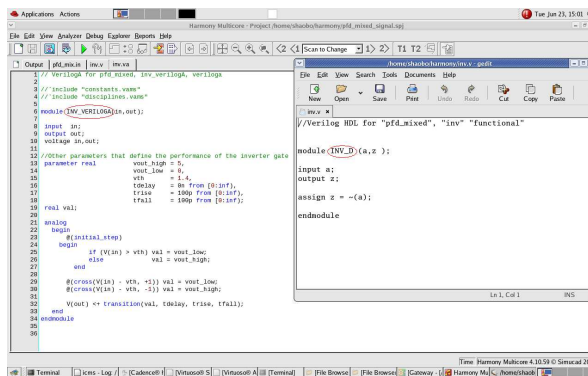


Figure 2-4

Finally, comment out stand C library constant and disciplines generated from Cadence in VerilogA (Figure 2-5) file and use default A2D D2A connection file since the power level definition is same as Spice VDD.

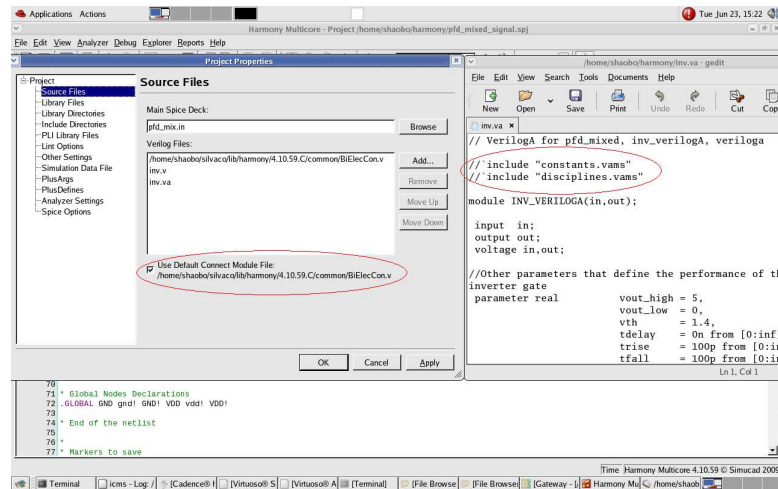


Figure 2-5

Harmony simulation (Figure 2-6) results match Cadence SpectreVerilog after a few minutes compilation.

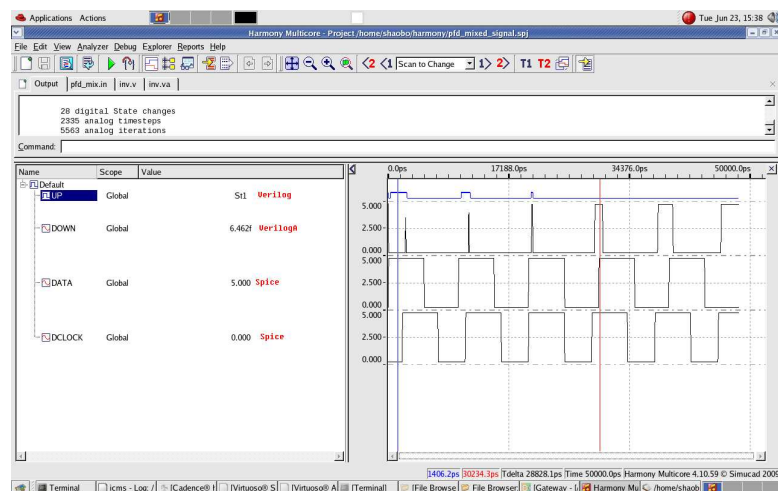


Figure 2-6

Conclusions

Cadence SpectreVerilog mixed signal simulation can be implemented in Simucad AMS design flow. Gateway directly loads Cadence EDIF 200, Cadence digital view such as Verilog, VerilogAMS and VerilogA is compatible to run under Harmony for mixed signal design. Simucad AMS also provides fast simulation timing and accurate simulation results.